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09/926,202	09/24/2001	Hiroshi Takeno	P107242-00024	6219

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EXAMINER	
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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Paper No. 05134

Application Number: 09/926,202
Filing Date: September 24, 2001
Appellant(s): TAKENO, HIROSHI

MAY 19 2004

Lynne D. Anderson
For Appellant

EXAMINER'S ANSWER

MAILED
MAY 19 2004
GROUP 1700

This is in response to the appeal brief filed 03/08/2004.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The brief does not contain a statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief. Therefore, it is presumed that there are none. The Board, however, may exercise its discretion to require an explicit statement as to the existence of any related appeals and interferences.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

The appellant's statement of the issues in the brief is correct.

(7) Grouping of Claims

The appellant's statement in the brief that certain claims do not stand or fall together is not agreed with because all claims are not addressed. Claims 7-9 are not described by the applicant as belonging to either group.

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,611,855	Wijaranakula	3-1997

Wolf et al., Silicon Processing for the VLSI Era Volume 1: Process Technology, Lattice Press, Sunset Beach, CA, USA, pp. 26-30, 59-61, 124, 133-136, 1986.

(10) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

1. Claims 6-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wijaranakula (5,611,855) in view of Wolf et al. (Silicon Processing for the VLSI Era Volume 1: Process Technology, Lattice Press, Sunset Beach, CA, USA, pp. 26-30, 59-61, 124, 133-136).

Wijaranakula discloses a method of making an epitaxial Si wafer with certain properties. The process is disclosed in col. 4 lines 15+. A doped (with boron, arsenic, antimony) Si substrate with a dissolved oxygen concentration of between 10-50 ppma (parts per million atoms) is used. Col. 5 lines 1-67 details the growth of an epitaxial layer on the wafer. The Si epitaxial wafer is annealed at between 600'C and 900'C to form oxygen microdefects in the wafer.

Wijaranakula does not disclose the deposition temperature of the epitaxial layer or the oxygen concentration in units of atoms/cm^3.

Wolf et al. discloses known Si physical properties. On page 59, the typical concentration of oxygen in Si is given as $5x10^{17}$ to $1x10^{18}$ atoms/cm^3 or 10-20 ppma. On page 135 it is disclosed than Si epitaxial growth is favored over etching in the range of temperatures from 900'C to 1400'C. Temperature optimization for annealing is disclosed on pages 60-61 and annealing from 650' to 750' C is discussed. On page 27 it is disclosed that Si doped with boron and antimony can have resistivities of from 0.005

ohm-cm upwards. Wolf et al. discloses the use of oxygen precipitates and denuded zones as gettering on page 61.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to combine Wijaranakula with Wolf et al. because Wolf discloses temperatures for epitaxial growth and annealing, a basis for comparing oxygen concentrations quoted in different units, resistivity of boron and antimony doped Si, and the known useful gettering action of oxygen precipitates in Si wafers.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to form a Si epitaxial wafer doped with boron (or antimony or arsenic) at a temperature of 1000'C or higher on a Si substrate having a oxygen concentration of $4x10^{17}$ to $10x10^{17}$ (equivalent to $1x10^{18}$)/cm3 and then heat treating the wafer at a temperature of from 450'C to 750'C because such is suggested by Wijaranakula in light of Wolf et al.

It would have been obvious to one of ordinary skill in the art at the time of the present invention that the resistivity of such a wafer would include the range of 0.02 ohm-cm or lower because such is disclosed by Wolf et al. for doped Si wafers and such resistivity was disclosed by Wolf et al. on page 26 as known to be a function of doping concentration.

It would have been obvious to one of ordinary skill in the art at the time of the present invention to optimize the process parameters including temperature such that oxygen precipitation nuclei were formed (thus increasing the bulk defect density) and not reducing the needed and well known use of the bulk Si oxygen precipitates for

gettering purposes because Wolf et al. discloses such use for oxygen precipitates in the bulk of Si wafers and temperatures for annealing such wafers.

(11) Response to Argument

Appellant's arguments filed in the brief have been fully considered but they are not persuasive.

In response to appellant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Wijaranakula discloses the basic Si epitaxial wafer with a specified oxygen concentration and a heat treatment to form oxygen precipitates. Wolf et al. gives equivalent units for oxygen concentration and further explains what the art knows to be true about gettering and doping in Si single crystals. The examiner gave this motivation in different terms above.

The argument that the oxygen concentration range and the epitaxial wafer heat treatment range are not merely optimized process parameters is not convincing. The appellants have not given any evidence of unexpected results and yet claims a method of forming an epitaxial wafer with the specified properties (i.e. oxygen concentration) annealed in a specific temperature range to give a wafer with gettering properties.

Gettering was completely expected in these ranges by those of ordinary skill in the art. The specific purpose cited was known in the art and also known to be accomplished in the ranges claimed.

The argument that there is no suggestion in the art to vary the substrate resistivity is not convincing. Wijaranakula discloses in col. 4 that the precipitation of oxygen can be practiced on substrates and epitaxial layers having wide ranges of thickness, dopants, and dopant concentrations. As an example, boron doping concentrations of $3x10^{18}$ atoms/cm^3 and $1x10^{15}$ atoms/cm^3 are given in col. 4 lines 30-45. Wolf et al. specifies that dopant concentration (i.e. impurity concentration) directly influences the resistivity of Si in Fig. 22 on page 28. This, and the specific range in Table 2 on page 27, would lead one of minimal skill in the art to conclude that Si with the doping concentration of Wijaranakula would have a resistivity of at least 0.005Ω-cm up to 50 Ω-cm. This range is suggested by Wolf in view of Wijaranakula depending on the dopant concentration present in the Si.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

MAA
May 17, 2004

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